REMARKS/AGRUMENTS

Reconsideration of this application, as amended, is respectfully requested. The following remarks are responsive to the Office Action mailed August 28, 2003.

Formal drawings are submitted, herewith.

Claims 1-27 are pending.

Claims 1-15 stand rejected.

Claims 16-42 have been added.

Claims10 and 13 have been amended. It is respectfully submitted that no new matter has been added.

Claims 1-15 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,110,217 of Kazmierski, et al., (hereafter, "Kazmierski").

CLAIM REJECTIONS – 35 USC §102 (e)

The Examiner rejected claims 1-15 under 35 U.S.C. §102(e) as being unpatentable over Kazmierski. Applicants submit that claims 1-15 are not anticipated by Kazmierski. In regard to the rejection of claim 1, the Examiner has stated in part that:

> Kazmierski et al. (217) teaches:...configuring said blocks in a block diagram structure; (col. 4, lines 34 et seq.) ordering said blocks in said block diagram structure to allow for waveform relaxation of sets of variables of said blocks; and performing waveform relaxation of said sets of variables of said blocks. (Office Action, 8/28/03, p. 4)

Applicant respectfully submits that claim 1is not anticipated by Kazmierski. Claim 1 recites the feature of "designing a controller with said blocks, and the relaxation variables, wherein the controller controls a system for manufacturing". (Emphasis added) This feature is

not disclosed by Kazmierski as shown by the following analysis. Kazmierski describes a system and method for synchronization of multiple analog servers on a simulation back plane. (Kazmierski, title) More specifically, Kazmierski simulates electrical circuits that are divided into sections. Each section has a section specific simulator module associated with it. The simulation modules communicate using block waveform relaxation. (Kazmierski, abstract) Kazmierski presents parallel processing circuit simulation to reduce the cost of integration of proprietary simulation engines and utility tools for circuit designers and electrical circuit CAD vendors. Thus, Kazmierski describes the use of circuit design tools and not a controller of a system for manufacturing. Kazmierski does not describe, "designing a controller with said blocks, and the relaxation variables, wherein the controller controls a system for manufacturing." Because, Kazmierski does not disclose this feature taught by applicants' claim 1, applicants respectfully submit that claim 1 and claims 2-14 which depend from claim 1 are not anticipated under 35 U.S.C. §102(e) by Kazmierski.

The Examiner also rejected in claim 15 under 35 U.S.C. §102(e) for the reasons set forth in the rejection of claim 1. Claim 15 discloses substantially similar features as claim 1, and recites "designing a controller with said blocks, and the relaxation variables, wherein the controller controls a system for manufacturing." (Emphasis added) Because, Kazmierski does not disclose these features as taught by applicants for the reasons discussed above with regard to claim 1, applicants respectfully submit that claim 15 is not anticipated under 35 U.S.C. §102(e) by Kazmierski.

For the foregoing reasons, applicant respectfully submits that the applicable objections and rejections have been overcome and that the claims are in condition for allowance. If there are any additional charges, please charge them to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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Sanjeet K. Dutta
Reg. No. 46,145

12400 Wilshire Blvd.
Seventh Floor
Los Angeles, CA 90025
(408) 947-8200